REMARKS/ARGUMENTS

Claims 1-3, 5, 7-14, 16-21 and 23 remain in the application, all of which stand rejected. Claims 4, 6, 15, 22 and 24 have been canceled, without prejudice.

Paragraph [0019] of the specification, and FIG. 3, have been amended without the addition of new matter.

Claim 1 has been amended to incorporate therein the limitations of canceled claim 6. Claims 10 and 11 have been amended so that they better conform to amended claim 1. Claim 14 has been amended similarly to claim 1. Claim 17 has been amended to incorporate therein the limitations of canceled claim 24. Claim 23 has been amended so that it better conforms to amended claim 17. None of these amendments are believed to add new matter.

1. Objection to the Specification

The Examiner objects to the specification due to a misspelling of "complementary" in paragraph [0019]. Appropriate correction has been made.

2. Objection to the Drawings

The Examiner objects to the drawings "because the black boxes in instant Fig. 3 need text labels." See, 1/13/2005 Office Action, sec. 2, p. 2.

Although applicants believe the reference numbers provided in FIG. 3 are sufficient to identify that which is disclosed (when combined with the corresponding description in paragraph [0017] of their specification), applicants submit herewith an amended FIG. 3 in which parts of the text description provided in their paragraph [0017] have been inserted. These amendments are not believed to add new matter.

3. Rejection of Claim 11 Under 35 USC 112, 2nd Paragraph

The Examiner asserts that, "Claim 11 is misdescriptive because the claim does not read on any of the disclosed embodiments, i.e., a single delay circuit with an output connected to the gates of the two (feedback) pull-up/pull-down FETs." See, 1/13/2005 Office Action, sec. 3, p. 3. Applicants respectfully disagree.

Applicants state in paragraph [0026]:

> And, if separate control over the positive and negative charge boost delays is not needed, the delay circuits 604, 608 may be merged into a common delay circuit (not shown).

Applicants believe this statement provides adequate support for their claim 11.

4. Rejection of Claims 1-3, 9, 13-17, 19 and 21-23 under 35 USC 102(b)

Claims 1-3, 9, 13-17, 19 and 21-23 stand rejected under 35 USC 102(b) as being anticipated by Williams et al. (US Pat. No. 3,798,471). In light of applicants' amendments to claims 1, 14 and 17, this rejection is believed to be moot.

5. Rejection of Claims 5, 7, 8, 12, 18 and 20 under 35 USC 103(a)

Claims 5, 7, 8, 12, 18 and 20 stand rejected under 35 USC 103(a) as being unpatentable over Williams et al. (US Pat. No. 3,798,471). In light of applicants' amendments to claims 1, 14 and 17, this rejection is believed to be moot.

6. Rejection of Claims 4, 6, 10, 11 and 24 under 35 USC 103(a)

Claims 4, 6, 10, 11 and 24 stand rejected under 35 USC 103(a) as being unpatentable over Hisaka (US Pat. No. 5,334,889) in view of Williams et al. (US Pat. No. 3,798,471). Applicants note that claim 6 has been incorporated into claim 1, and claim 24 has been incorporated into claim 17 (so the Examiner's rejections of claims 6 and 24 now respectively apply to claims 1 and 17).

The Examiner asserts:

> As to claims 4, 6 and 24, note Fig. 1 of Hisaka, which shows a first switching circuit (the PFET within inverter 13), a first current clamp (R10), a delay circuit (inverters 14 and 15) and a FET (Tr15) is parallel with the resistor. Not shown is the parallel capacitor but such would have been obvious in view of the above-noted teachings of Williams et al. The motivation for adding such a capacitor in parallel with the resistor R10 is to increase the switching speed of the PFET within inverter 13 (as taught by Williams et al).

1/13/2005 Office Action, sec. 6, p. 6.

Applicants respectfully disagree. Although Hisaka teaches FET (Tr15) in parallel with resistor (R10), applicants note that Hisaka's FET (Tr15) is not part of a "non-persistent charge boost circuit", as is the FET recited in applicants' claims 1 and 17. Hisaka states:

> As the level of the input signal S11, which is applied to the input electrode of the inverter circuit 13, shifts from a high to low level in the output buffer circuit of the above-described construction at a moment t0 as shown in (A) of FIG. 2, an output node n13 of the inverter circuit 13 rises from earth to the power source level as shown in (B) of FIG. 2. Since the fourth and fifth transistors Tr14, Tr15 are both in an off-state at this moment, the rising time of the node 13 takes an integrated form due to operation of the resistor R10 and the capacitor C10 and the voltage of the node n13 rises gradually as illustrated in (B) of FIG. 2.

Hisaka, col. 3, lines 20-31.

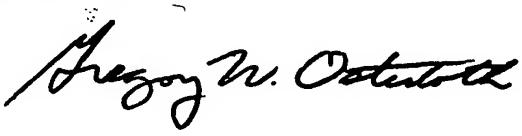
Thus, Hisaka's FET (Tr15) operates differently, and performs a different function, than the FET recited in applicants' claims 1 and 17.

Applicants' claims 1 and 17 are therefore believed to be allowable over Hisaka's and Williams et al's combined teachings. Claims 2, 3, 5, 7-14, 16, 18-21 and 23 are believed to be allowable because they depend from one of claims 1 or 17, or for reasons similar to why claims 1 and 17 are believed to be allowable.

7. Conclusion

In light of the amendments and remarks provided herein, applicants respectfully request the timely issuance of a Notice of Allowance.

Respectfully submitted,
DAHL & OSTERLOTH, L.L.P.



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Amendments to the Drawings:

The attached sheet of drawings includes changes to FIG. 3. This sheet, which only includes FIG. 3, replaces the original sheet including FIG. 3. In FIG. 3, text labels have been added to the boxes illustrated therein.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

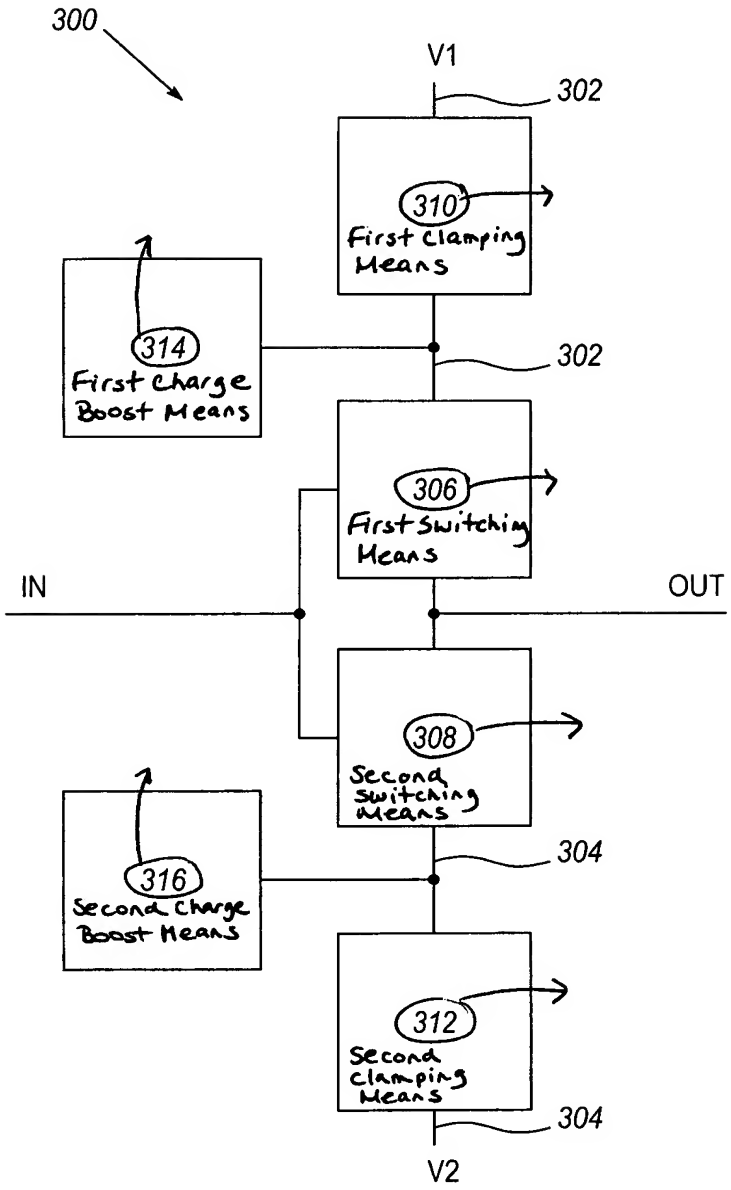

FIG. 3